As to the Objection to the Drawings:

The Examiner has objected to the drawings for not showing (a) the solder containing compound and (b) the pick and place tool.

The Applicant has canceled claim 5 from the application, thus rendering moot the objection as to the drawings not depicting the pick and place tool.

As to the objection to the drawings for not rendering the solder containing compound, the Applicant first draws the Examiner's attention to the guiding statute which states that a drawing is required where a drawing is necessary for an understanding of the invention. (35 U.S.C. § 113.)

Further, the Applicant draws the Examiner's attention to MPEP 601.01(f) which states that it has been USPTO practice to treat an application that contains at least one process or method claim as an application for which a drawing is not necessary for an understanding of the invention under 35 U.S.C. § 113 (first sentence).

The Applicant notes that other situations in which drawings are usually not considered necessary for an understanding include those where a coating is applied. The part of the claims at issue here that have brought to the Examiner's attention the issue of drawings (other than the already treated issue of the pick and place machine) is the application of a solder-containing compound to members of a carrier frame. As the Affidavit of James G. Wilder Under 37 CFR § 1.132 (the "Wilder Affidavit") points out, the application of solder paste is an instance of applying a solder containing compound to the carrier frame. The Wilder Affidavit further shows that no drawing is necessary to understand this feature of the claims. The application of a solder paste is in the nature of applying a coating, one of the instances in the MPEP where a drawing has not been considered required.

Thus, in light of the Wilder Affidavit and the MPEP, the Applicant here believes that no new drawings are required for the application in light of the cancellation of claim 5 and requests that the drawings be accepted.

As to the Objection to the Specification:

The specification has been objected to for lack of clarity as to the antecedent basis for the "multiple iterations" and "indents" terms.

The Applicant has canceled claim 4, thus rendering moot the objection as to the term "indents."

The Applicant notes that the Examiner rejects claim 2 for use of the term "multiple" and states that such a term renders the claim indefinite. Although the Applicant does not agree, in the interest of moving the case toward allowance, the Applicant has amended claim 2 by replacing "multiple" with "plural." Thus, the objection to the specification as to "multiple" is resolved by that amendment.

The Applicant now refers the Examiner to Fig. 11 of the application where there are clearly shown plural iterations of the carrier frame. Thus, in light of the amendments made here, and the Wilder Affidavit, the Applicant believes the specification to be non-objectionable.

As to the Claim Rejections under 35 U.S.C. § 112.

The Applicant has amended claims 1-3 and believes that, in the additional light of the Wilder Affidavit, the amendments herein have resolved the issues presented by the Examiner as to Section 112 and that, therefore, claims 1-3 are proper under 35 U.S.C. § 112.

Thus, in light of the Wilder Affidavit and the MPEP, the Applicant here believes that no new drawings are required for the application in light of the cancellation of claim 5 and requests that the drawings be accepted.

As to the Objection to the Specification:

The specification has been objected to for lack of clarity as to the antecedent basis for the "multiple iterations" and "indents" terms.

The Applicant has canceled claim 4, thus rendering moot the objection as to the term "indents."

The Applicant notes that the Examiner rejects claim 2 for use of the term "multiple" and states that such a term renders the claim indefinite. Although the Applicant does not agree, in the interest of moving the case toward allowance, the Applicant has amended claim 2 by replacing "multiple" with "plural." Thus, the objection to the specification as to "multiple" is resolved by that amendment.

The Applicant now refers the Examiner to Fig. 11 of the application where there are clearly shown plural iterations of the carrier frame. Thus, in light of the amendments made here, and the Wilder Affidavit, the Applicant believes the specification to be non-objectionable.

As to the Claim Rejections under 35 U.S.C. § 112.

The Applicant has amended claims 1-3 and believes that, in the additional light of the Wilder Affidavit, the amendments herein have resolved the issues presented by the Examiner as to Section 112 and that, therefore, claims 1-3 are proper under 35 U.S.C. § 112.

As to the Claim Rejections under 35 U.S.C. § 103.

Claims 1-4 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Hikita et al (U.S. Pat. No. 6,133, 637, hereafter, "*Hikita*") in view of Sakai et al., U.S. Pat. No. 5,894,984, hereafter, "*Sakai*"). The present cancellation of claim 4 renders moot the rejection as to claim 4. The Applicant believes that in light of the amendments made herein, the claims 1-3 are in condition for allowance and remarks as follows:

The Applicant initially notes that the cited primary reference *Hikita* is directed to aggregating semiconductor die within a single package. For example, after describing an affixation of the two IC chips 14 and 16 to a leadframe 12, *Hikita* describes a transfer-molded encapsulation of the entirety of chips 14 and 16 into a single package. (Col. 21, lines 11-14.)

In contrast to *Hikita*, the present invention does not aggregate unpackaged IC chips and does not, despite what seems to be such a characterization by the Examiner, form or relate to forming an encapsulating member to protect an integrated circuit device. (See Office action page 6, paragraph 14.) The Applicant refers the Examiner to the drawings herein and notes that there is no transfer molding step involved in the present invention. The Applicant does not understand the Examiner's reference to transfer molding as a suggested commonality to tie the cited references *Hikita* and *Sakai* to the claimed invention. Even so, the Applicant has amended the claims to make more clear the subject matter that the Applicant regards as his invention.

The present invention disposes an *already packaged* IC on the members of a carrier frame for connection. As is clear from the amendment made herein, the present invention of this application claims subject matter related to aggregating already packaged integrated circuits.

Thus, to the degree that *Hikita* teaches appending bare die to lead frames and subsequent transfer molding operations, it is inapposite to the present invention. Further, the secondary

reference *Sakai*, teaches methods related to soldering and use of solders with melting points greater than a thermal deformation temperature of a board to which the device is to be mounted, subject matter that is not addressed by the Applicant's invention.

Even if *Hikita* and *Sakai* were combined (and the Applicant further notes there is no such suggestion in either reference), the present invention would not be rendered. First, the primary reference teaches methods related to packaging two die into a single package. In contrast, the present invention aggregates two *already packaged* integrated circuits into a circuit module. Secondly, the issues of solder temperature and transfer molding are not addressed by the present invention and thus, where the *Sakai* reference is relied upon by the Examiner for its description of heat application in a transfer molding operation, a processing step not even remotely related to the present invention is described.

Even though the Applicant does not see the relevance of the Examiner's offered Section 103 references to the present invention, it has amended its claims to more clearly claim the subject matter regarded to be the invention.

Consequently, the Applicant has amended the present claim 1 and by dependency therefore, claims 2 and 3, to more clearly recite the claimed subject matter. In light of the amendments made herein, the Applicant believes claims 1-3 to be patentable and respectfully requests an indication of allowance at the earliest opportunity.

Attached are sheets showing the claims with changes made and sheets showing the claims after entry of the amendments made herein.

Respectfully submitted,

ANDREWS & KURTH, L.L.P.

Date: April 22, 2003

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Claims Version Showing Changes Made by Present Amendment

1. (Amended) A method of creating a stack of integrated circuits selectively connected to provide increased memory density in an application, the method comprising the steps of: providing a carrier frame configured to have a plurality of members emergent into a window within the carrier frame; applying a solder-containing compound to the first side of the plurality of members; placing a first packaged integrated circuit in contact with the plurality of members; processing [the combination of] the first integrated circuit and the carrier frame with a heat source to create solder connections between the plurality of members and the first packaged integrated circuit; applying a solder-containing compound to the second side of the plurality of members of the carrier frame; placing a second packaged integrated circuit in contact with the plurality of members; processing [the combination of] the [first] second integrated circuit and the carrier frame with a heat source to create solder connections between the plurality of members and the second integrated circuit.

2. (Amended) The method of claim1 in which [multiple] plural iterations of the carrier frame are created in a carrier bed.

3. (Amended) The method of claim 1 in which [the resulting assembly of] the carrier frame and the first and second integrated circuits [is] are further processed by separation of the plurality of members from the carrier frame.

Claims as Amended

1. A method of creating a stack of integrated circuits selectively connected to provide increased memory density in an application, the method comprising the steps of: providing a carrier frame configured to have a plurality of members emergent into a window within the carrier frame; applying a solder-containing compound to the first side of the plurality of members; placing a first packaged integrated circuit in contact with the plurality of members; processing the first integrated circuit and the carrier frame with a heat source to create solder connections between the plurality of members and the first packaged integrated circuit; applying a solder-containing compound to the second side of the plurality of members of the carrier frame; placing a second packaged integrated circuit in contact with the plurality of members; processing the second integrated circuit and the carrier frame with a heat source to create solder connections between the plurality of members and the second integrated circuit.

2. The method of claim 1 in which plural iterations of the carrier frame are created in a carrier bed.

3. The method of claim 1 in which the carrier frame and the first and second integrated circuits are further processed by separation of the plurality of members from the carrier frame.